LISTING OF CLAIMS

This Listing of Claims replaces all prior versions and listings of the claims in this application.

1. (currently amended) A fractional-N phase-locked loop, comprising:

a phase detector, comprising:

a first input that receives a first signal;

a second input that receives a second signal; and

a comparison circuit that generates a phase detector output signal that is a function of a phase difference between the first signal and the second signal;

a loop filter that generates a frequency control signal from the phase detector output signal,

a circuit that generates a phase-locked loop output signal having a frequency that is controlled by the frequency control signal,

a frequency divider that generates the second signal from the phase-locked loop output signal,

a sigma-delta modulator that generates division values for the frequency divider, and

an operating point circuit that maintains an operating point of the phase detector at a position with a nonzero output signal and a corresponding nonzero phase difference between the first and second signals, such that for a predetermined range of both positive and negative phase differences between the first and second signals, the output signal is generated as a substantially linear function of the phase difference between the first signal and the second signal, wherein the substantial linearity of the output signal is due at least in part to a shifting of the operating point so that a nonzero output signal corresponds to a nonzero phase difference between the first and second signals, and the nonzero phase difference is close to or larger than an amount of time equal to at least a number of cycles of the phase-locked loop output signal.

2. (currently amended) The fractional-N phase-locked loop of claim 1, wherein the ~~nonzero phase difference of the operating point is close to or larger than an amount of time equal to a number of cycles of the second signal~~ amount of time is such that

delta-sigma ($\Delta\Sigma$) noise is confined to one side of a zero-crossing of the phase detector output signal.

3. (previously presented) The fractional-N phase-locked loop of claim 1, wherein the phase detector output signal is an output current; and wherein the comparison circuit comprises:

a first circuit that asserts a first charge pump control signal in response to an edge of the first signal;

a second circuit that asserts a second charge pump control signal in response to an edge of the second signal;

a first charge pump that contributes a positive current to the output current in response to assertion of the first charge pump control signal;

a second charge pump that contributes a negative current to the output current in response to assertion of the second charge pump control signal; and

reset logic that supplies a reset signal to each of the first and second circuits in response to both of the first and second charge pump control signals being asserted, and

wherein the operating point circuit comprises:

a delay circuit that delays at least one of the first and second charge pump control signals from being supplied to the reset logic, wherein a length of time that it takes the first charge pump control signal to be supplied to the reset logic is not equal to the length of time that it takes the second charge pump control signal to be supplied to the reset logic.

4. (previously presented) The fractional-N phase-locked loop of claim 3, wherein the delay circuit delays only one of the first and second charge pump control signals from being supplied to the reset logic.

5. (previously presented) The fractional-N phase-locked loop of claim 3, wherein the delay circuit delays both the first and second charge pump control signals from being supplied to the reset logic.

6. (previously presented) The fractional-N phase-locked loop of claim 1, wherein the phase detector output signal is an output voltage; and wherein the comparison circuit comprises:

a first circuit that asserts a first voltage generator control signal in response to an edge of the first signal;

a second circuit that asserts a second voltage generator control signal in response to an edge of the second signal;

a first voltage generator that contributes a positive voltage to the output voltage in response to assertion of the first voltage generator control signal;

a second voltage generator that contributes a negative voltage to the output voltage in response to assertion of the second voltage generator control signal; and

reset logic that supplies a reset signal to each of the first and second circuits in response to both of the first and second voltage generator control signals being asserted, and

wherein the operating point circuit comprises:

a delay circuit that delays at least one of the first and second voltage generator control signals from being supplied to the reset logic, wherein a length of time that it takes the first voltage generator control signal to be supplied to the reset logic is not equal to the length of time that it takes the second voltage generator control signal to be supplied to the reset logic.

7. (previously presented) The fractional-N phase-locked loop of claim 6, wherein the delay circuit delays only one of the first and second voltage generator control signals from being supplied to the reset logic.

8. (previously presented) The fractional-N phase-locked loop of claim 6, wherein the delay circuit delays both the first and second voltage generator control signals from being supplied to the reset logic.

9. (currently amended) A fractional-N phase-locked loop comprising:

a phase detector that comprises:

a first input that receives a reference clock signal; a second input that receives a feedback signal; and

a comparison circuit that generates a phase detector output signal that is a function of a phase difference between the reference clock signal and the feedback signal;

an operating point circuit that maintains an operating point of the phase detector at a position with a nonzero output signal and corresponding nonzero phase difference between the reference clock and feedback signals, such that for a predetermined range of both positive and negative phase differences between the reference clock and feedback signals, the output signal is generated as a substantially linear function of the phase difference between the reference clock and feedback signals, wherein the substantial linearity of the output signal is due at least in part to a shifting of the operating point so that a nonzero output signal corresponds to a nonzero phase difference between the reference clock and feedback signals<u>, and the nonzero phase difference is close to or larger than an amount of time equal to at least a number of cycles of a phase-locked loop output signal</u>;

a loop filter that generates a frequency control signal from the phase detector output signal;

a circuit that generates [[a]] <u>the</u> phase-locked loop output signal that has a frequency that is controlled by the frequency control signal;

a frequency divider that generates the feedback signal from the phase-locked loop output signal;

a sigma-delta modulator that generates division values for the frequency divider; and

one or more circuit elements that leak a predefined portion of at least one of the phase detector output signal and the frequency control signal so as to prevent the leaked signal from influencing the output frequency of the phase-locked loop.

10. (original) The phase-locked loop of claim 9, wherein the one or more circuit elements that leak a predefined portion of at least one of the phase detector output signal and the frequency control signal comprise:

one or more circuit elements in the loop filter that leak a predefined portion of the phase detector output signal.

11. (original) The phase-locked loop of claim 9, wherein the circuit that generates the phase-locked loop output signal that has a frequency that is controlled by the frequency control signal is a voltage controlled oscillator.

12. (original) The phase-locked loop of claim 9, wherein the circuit that generates the phase-locked loop output signal that has a frequency that is controlled by the frequency control signal is a current controlled oscillator.

13. (currently amended) A method of generating a fractional-N phase-locked loop output signal, the method comprising:

generating a phase detector output signal that is a function of a phase difference between a first signal and a second signal;

maintaining an operating point at a position with a nonzero output signal and a corresponding nonzero phase difference between the first signal and the second signal, such that for a predetermined range of both positive and negative phase differences between the first and second signals, the output signal is generated as a substantially linear function of the phase difference between the first signal and the second signal, wherein the substantial linearity of the output signal is due at least in part to a shifting of the operating point so that a nonzero output signal corresponds to a nonzero phase difference between the first and second signals, and the nonzero phase difference is close to or larger than an amount of time equal to at least a number of cycles of the phase-locked loop output signal;

generating a frequency control signal from the phase detector output signal;

generating the phase-locked loop output signal having a frequency that is controlled by the frequency control signal;

using a frequency divider to generate the feedback signal from the phase-locked loop output signal; and

using a sigma-delta modulator to generate division values for the frequency divider.

14. (currently amended) The method of claim 13, wherein the ~~nonzero phase difference of the operating point is greater than or substantially equal to an amount of time equal to a number of cycles of the second signal~~ amount of time is such that delta-

<u>sigma ($\Delta\Sigma$) noise is confined to one side of a zero-crossing of the phase detector output signal</u>.

15. (original) The method of claim 13, wherein

the output signal is an output current; and

wherein the step of generating the output signal that is a function of the phase difference between the first signal and the second signal comprises:

asserting a first charge pump control signal in response to an edge of the first signal;

asserting a second charge pump control signal in response to an edge of the second signal;

contributing a positive current to the output current in response to assertion of the first charge pump control signal;

contributing a negative current to the output current in response to assertion of the second charge pump control signal; and

deactivating the first and second charge pump control signals in response to both of the first and second charge pump control signals being asserted, and

wherein the step of maintaining the operating point of the phase detector comprises:

delaying at least one of the first and second charge pump control signals from affecting the deactivating step, wherein a length of time that it takes the first charge pump control signal to affect the deactivating step is not equal to the length of time that it takes the second charge pump control signal to affect the deactivating step.

16. (original) The method of claim 15, wherein the step of delaying comprises delaying only one of the first and second charge pump control signals from affecting the deactivating step.

17. (original) The method of claim 15, wherein the step of delaying comprises delaying both the first and second charge pump control signals from affecting the deactivating step.

18. (original) The method of claim 13, wherein the output signal is an output voltage; and

wherein the step of generating the output signal that is a function of the phase difference between the first signal and the second signal comprises:

asserting a first voltage generator control signal in response to an edge of the first signal;

asserting a second voltage generator control signal in response to an edge of the second signal;

contributing a positive voltage to the output voltage in response to assertion of the first voltage generator control signal;

contributing a negative voltage to the output voltage in response to assertion of the second voltage generator control signal; and

deactivating the first and second voltage generator control signals in response to both of the first and second voltage generator control signals being asserted, and

wherein the step of maintaining the operating point of the phase detector comprises:

delaying at least one of the first and second voltage generator control signals from affecting the deactivating step, wherein a length of time that it takes the first voltage generator control signal to affect the deactivating step is not equal to the length of time that it takes the second voltage generator control signal to affect the deactivating step.

19. (original) The method of claim 18, wherein the step of delaying comprises delaying only one of the first and second voltage generator control signals from affecting the deactivating step.

20. (original) The method of claim 18, wherein the step of delaying comprises delaying both the first and second voltage generator control signals from affecting the deactivating step.

21. (currently amended) A method of generating a fractional-N phase-locked loop output signal, comprising:

generating a phase detector output signal that is a function of a phase difference between a reference clock signal and a feedback signal;

maintaining an operating point at a position with a nonzero output signal and a corresponding nonzero phase difference between the reference clock signal and the feedback signal, such that for a predetermined range of both positive and negative phase differences between the reference clock and feedback signals, the output signal is generated as a substantially linear function of the phase difference between the reference clock and feedback signals, wherein the substantial linearity of the output signal is due at least in part to a shifting of the operating point so that a nonzero output signal corresponds to a nonzero phase difference between the reference clock and feedback signals, and the nonzero phase difference is close to or larger than an amount of time equal to at least a number of cycles of the phase-locked loop output signal;

generating a frequency control signal from the phase detector output signal;

generating the phase-locked loop output signal that has a frequency that is controlled by the frequency control signal;

using a frequency divider to generate the feedback signal from the phase locked loop output signal;

using a sigma-delta modulator to generate division values for the frequency divider; and

leaking a predefined portion of at least one of the phase detector output signal and the frequency control signal so as to prevent the leaked signal from influencing the output frequency of the phase-locked loop.

22. (original) The method of claim 21, wherein the step of leaking a predefined portion of at least one of the phase detector output signal and the frequency control signal comprises:

leaking a predefined portion of the phase detector output signal in a loop filter.